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SJPME Yale, N Patt - doi.ieeecomputersociety.org

... The instruction may be stored in multiple locations in the **trace cache**.

Figure 8 shows a **loop** composed of three fetch blocks. ...

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[Critical Issues Regarding the Trace Cache Fetch Mechanism - group of 3 »](#)

SJ Patel, DH Friendly, YN Patt - Ann Arbor - cs.wpi.edu

... in a greedy fashion, there are cases where the ll unit can create multiple copies of basic blocks in the **trace cache**. Figure 3 shows a simple **loop** composed of ...

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E Rotenberg, S Bennett, JE Smith - IEEE Transactions on Computers, 1999 - doi.ieeeecs.org

... Trace selection primarily affects average trace length and **trace cache** hit rate, both ... techniques that are conscious of control flow constructs—**loop** back-edges ...

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[Evaluation of Design Options for the Trace Cache Fetch Mechanism - group of 15](#)

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SJ Patel, DH Friendly - Evaluation, 1999 - doi.ieeeecs.org

... unit can potentially create five different trace segments containing portions of this **loop**, all of which can be simultaneously resident in the **trace cache**. ...

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[Software Trace Cache - group of 12 »](#)

A Ramirez, JL Larriba-Pey, M Valero - IEEE Transactions on Computers, 2005 - doi.ieeecomputersociety.org

... The Software **Trace Cache** (STC) layout algorithm is largely based on the work of ... The algorithm follows the most likely path through the **loop** body until the ...

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R Rosner, A Mendelson, R Ronen - Parallel Architectures and Compilation Techniques, 2001. ..., 2001 - ieeexplore.ieee.org

... o that the LU mechanisms tries to fit a maximal number of whole **loop**-iterations into a ... **Trace-Cache** Organization A **trace cache** consists of controls and data area ...

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[A 0.18  \$\mu\$ m CMOS IA32 microprocessor with a 4 GHz integer execution unit - group of 2 »](#)

D Sager, G Hinton, M Upton, T Chappell, TD ... - Solid-State Circuits Conference, 2001. Digest of Technical ..., 2001 - ieeexplore.ieee.org

... than 70% of dynamic instructions in typical integer programs use this integer ALU **loop**, reducing this ... The system bus logic and execution **trace cache** run at 1GHz ...

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[Control Independence in Trace Processors - group of 43 »](#)

E Rotenberg, J Smith - Proceedings of the 32nd annual ACM/IEEE international ..., 1999 -

doi.ieeecomputersociety.org

... a large number of small traces, worsen- ing PE utilization, **trace cache** performance, and ... **Loop** back-edges, **loop** exits, and subroutine return points are all ...

[Cited by 291](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Improving dynamic cluster assignment for clustered \*\*trace cache\*\* processors - group of 9 »](#)

R Bhargava, LK John - Computer Architecture, 2003. Proceedings. 30th Annual ..., 2003 - [ieeexplore.ieee.org](#)

... 4.2. Dynamic Instruction Feedback The **trace cache** framework provides a unique instruc- tion feedback **loop**. Instructions are fetched ...

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[\[book\] Speculative multithreaded processors - group of 35 »](#)

P Marcuello, A González, J Tubella - 1998 - ACM Press New York, NY, USA

... increase, it could be supported by a special single-ported cache, which we call **loop cache** (see Figure 8) that has some similarities with the **trace cache** [IS]. ...

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R Rosner, A Mendelson, R Ronen - Parallel Architectures and Compilation Techniques, 2001. ..., 2001 - [ieeexplore.ieee.org](#)

... build mechanism employs simple **loop unrolling** heuristics and ... a maximal number of whole **loop**-iterations into ... **Trace-Cache** Organization A **trace cache** consists of ...

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V Bala, E Duesterwald, S Banerjia - Proceedings of the ACM SIGPLAN 2000 conference on ..., 2000 - [portal.acm.org](#)

... Other conventional optimizations performed are copy propagation, constant propagation, strength reduction, **loop** invariant code motion and **loop unrolling**. ...

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C Young, MD Smith - Proceedings of the 31st annual ACM/IEEE international ..., 1998 - [doi.ieeeecomputersociety.org](#)

... The IMPACT designers list three distinct superblock- enlarging optimizations: branch target expansion, **loop** peel- ing, and **loop unrolling** [8]. In branch target ...

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[Increasing the size of atomic instruction blocks using control flow assertions - group of 6 »](#)

SJ Patel, T Tung, S Bose, MM Crum - Proceedings of the 33rd annual ACM/IEEE international ..., 2000 - [portal.acm.org](#)

... a high level (-O4) of opti- mization including function in- lining and **loop unrolling**. ...

Much of this work builds upon previous **trace cache** research [11, 12, 9 ...

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... Since **unrolling** may significantly boost fetch bandwidth for a small **loop**, the benefit ...

The per- centage increase is over a **trace cache** which performs ...

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A Ramirez, JL Larriba-Pey, M Valero - IEEE Transactions on Computers, 2005 - [doi.ieeeecomputersociety.org](#)

... We optimize the code layout using the Software **Trace Cache** (STC) algorithm, which ... **loop** terminations cannot be reversed (unless we perform **loop unrolling**) 2 and ...

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SJ Patel, SS Lumetta - Computers, IEEE Transactions on, 2001 - [ieeexplore.ieee.org](#)

... Much of this work builds upon previous **trace cache** research [24], [25], [22], in ...

C Compiler V3.5 at the maximum optimization level (including **loop unrolling**). ...

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[The performance of runtime data cache prefetching in a dynamic optimization system - group of 8 »](#)

J Lu, H Chen, R Fu, WC Hsu, B Othmer, PC Yew, DY ... - Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual ..., 2003 - [ieeexplore.ieee.org](#)

... in this exam- ple exhibit unit stride, the compiler could **unroll** the **loop** to ... cache prefetch optimizations only for the code re- gion/**loop** that has ... **Trace Cache** ...

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[Design and implementation of a lightweight dynamic optimization system - group of 3 »](#)

J Lu, H Chen, PC Yew, WC Hsu - Journal of Instruction-Level Parallelism, 2004 - jilp.org  
... of executing the alloc itself after deploying the trace into the **trace cache** (ie  
the ... over five times faster on an Itanium 2 machine) by using **loop unrolling**. ...  
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R Rosner, M Moffie, Y Sazeides, R Ronen - Proceedings of the 17th annual international conference on  
..., 2003 - portal.acm.org

... and novel dynamic selection approaches – including **loop unrolling**, procedure in ... Keywords

Trace processors, **trace cache**, trace selection, trace atomicity. ...

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